Title: Logic Circuit with Restrained Leak ...

Inventor: Yasushi Amamiya App. Ser. No.: 10/560,930 Atty. Dkt. No.: 040373-0367

Fig. 1 (Prior Art)

Replacement Sheet

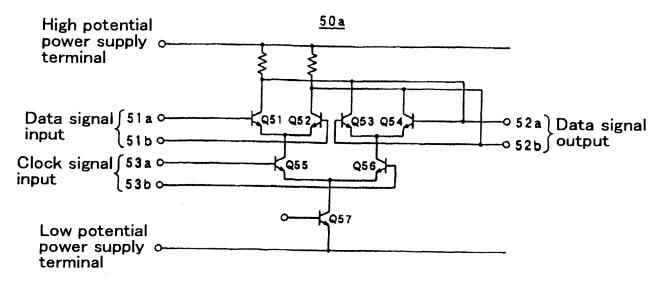


Fig. 2 (Prior Art)

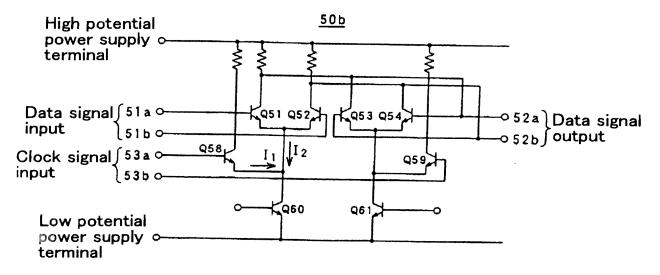
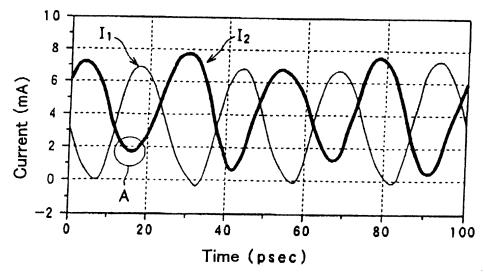


Fig. 3 (Prior Art)



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Fig. 4 (Prior Art)

Replacement Sheet

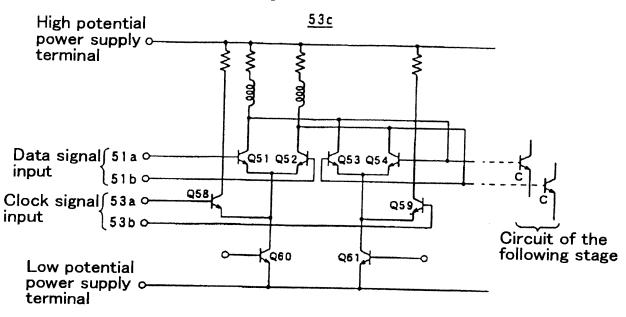


Fig. 5 (Prior Art)

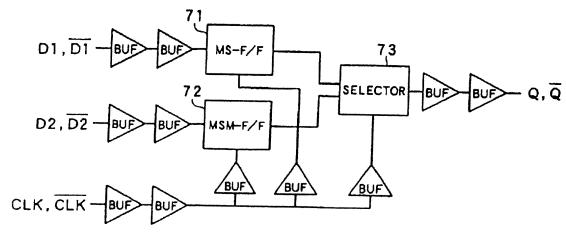


Fig. 6

